Abstract

A signal delaying device (1) for the dynamic delaying of a digitally sampled input signal comprises a memory element (2) and a series-connected interpolation element (3). According to the invention, a register (30), which can be connected to the output side of the interpolation element (3), is arranged in parallel to the memory element (2) for intermediate storage of at least one sampled value ($S_{in}(k)$) of the input signal.

(Figure 2)